Instructions

Tektronix

Training Board 2
Demonstration Board for Oscilloscopes, Logic Analyers, and Probes

071-1137-00

This document applies to firmware version 1.1 and above.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Symbols on the Product. The following symbols may appear on the product:

CAUTION
Refer to Manual

Protective Ground
(Earth) Terminal

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Contacting Tektronix

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Address	Tektronix, Inc. Department or name (if known) 14200 SW Karl Braun Drive P.O. Box 500 Beaverton, OR 97077 USA
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*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

General Information

Training and Demonstration Board for High Performance Oscilloscopes, Logic Analyzers and Probes. Training Board 2 generates signals that demonstrate features for high performance electrical and optical oscilloscopes, logic analyzers and probes.

Figure 1: Tektronix training board 2

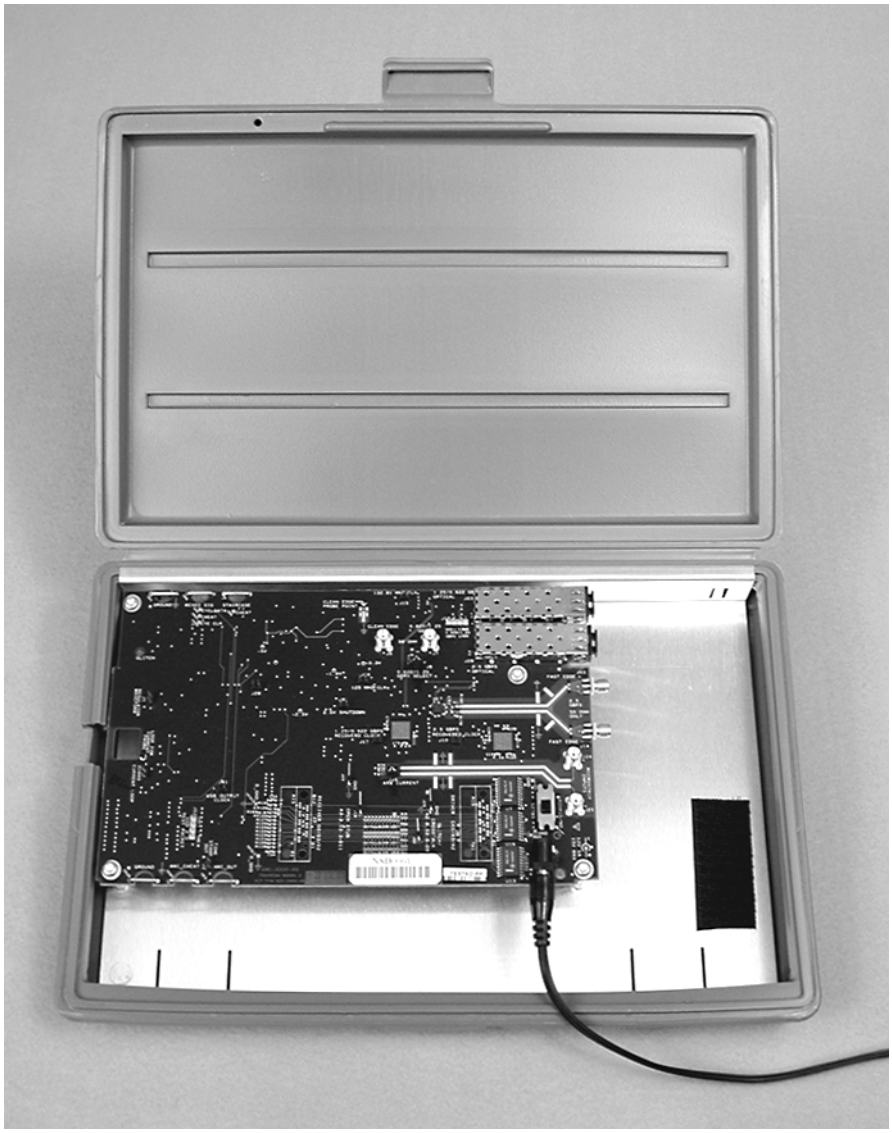


Figure 2: Training and demonstration board

Overall Description

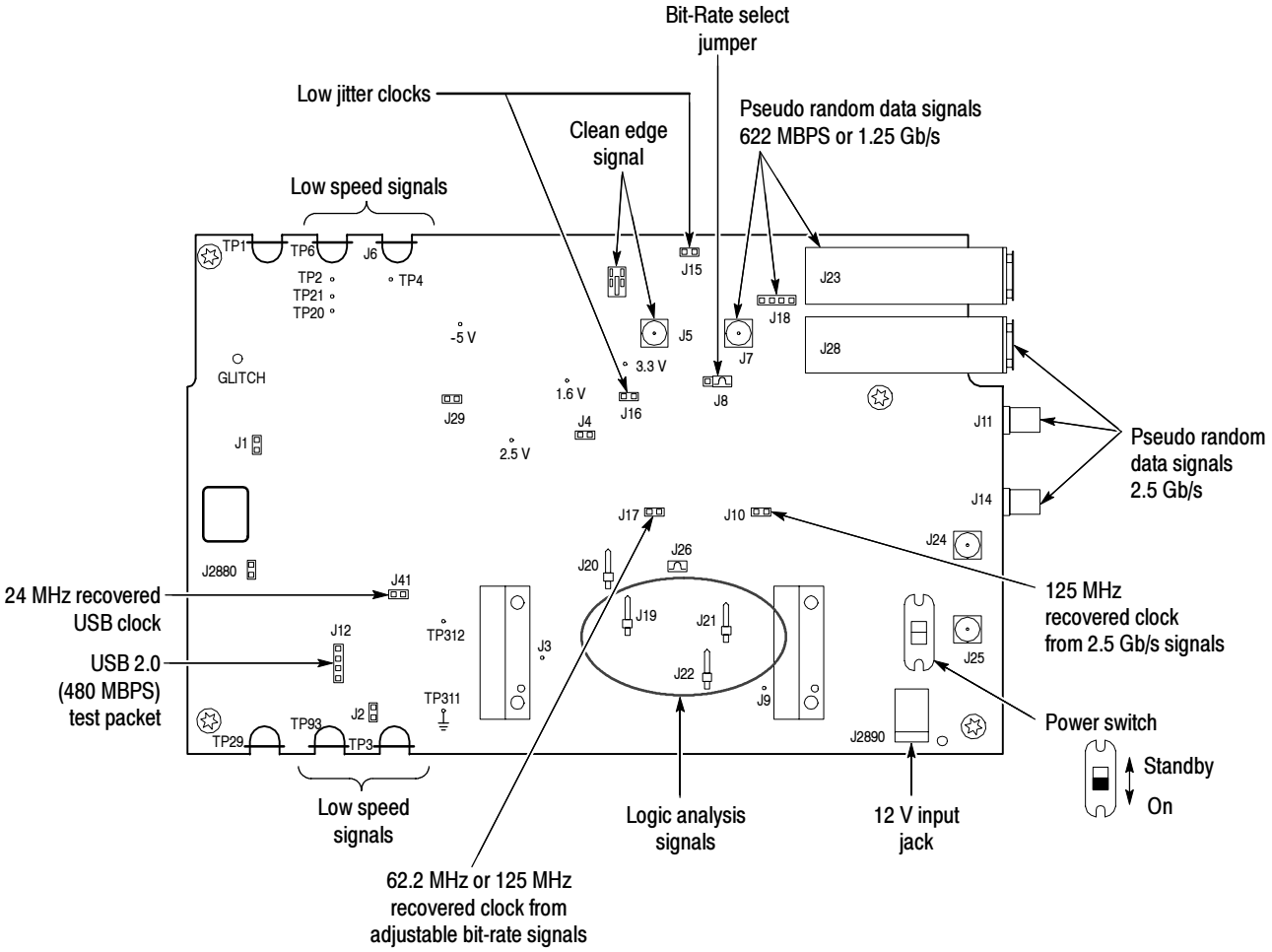


Figure 3: Training Board 2 signal and test points

Signals

The following signals are available on Training Board 2:

Table 1: Signal Specifications

Signal		Specification
J1	Switching power supply voltage signal	Approximately ±5V square wave at approximately 270 kHz amplitude and frequency depend on power supply loading.
3.3 V	3.3 V power supply test point	3.3V ±5%
1.6 V	1.6 V power supply test point	1.2 V to 2.0 V
2.5 V	2.5 V power supply test point	2.5 V ±5%
-5 V	-5 V power supply test point	-5.0 V ±5%
TP1	Ground test point	
TP29	Ground test point	
J6	Staircase waveform with glitches.	Frequency: 700 Hz Amplitude 4.0 Vpp.
TP4	Staircase “cheat” signal	Positive TTL pulse that signifies a waveform glitch on the staircase waveform.
J29	External reference for Clean Edge	TTL input, R762 must be removed and R761 must be installed.
J5	Clean Edge Output including a probing point.	-0.25 V baseline steps to 0 V with a risetime between 200 ps and 300 ps. Falltime is between 5 ns and 10 ns. Source impedance is 50 ohms.
J8	1.25 Gb/s or 0.625 Gb/s select jumper	Select as marked on board.
J24 and J25	External signal input..	Intended to be used with an arbitrary waveform generator. It allows connections to probes.
J26	Current probe jumper	Disconnect to insert a current probe.
J7	1.25 Gb/s or 0.625 Gb/s output	Output level is LVPECL minus 1.2 V.
J18	LVDS Output	LVDS voltage levels at J7’s output data rate. Insertion of optical module affects output - the least overshoot occurs with the module installed.
J23	1.25 Gb/s or 0.625 Gb/s optical module	Insert appropriate module such as the SFP size optical transceiver.
J11 and J14	Fast Edge Output	Vol = 700 mV, Voh = 1.1 V (RSECL output minus 0.5 V) at a 2.5 Gb/s data rate. Edge rate is less than 50 ps (20% to 80%).
J28	2.5 Gb/s optical module	Insert appropriate module such as the SFP size optical transceiver.

Table 1: Signal Specifications (Cont.)

Signal		Specification
TP6	Random Anomalies (Mixed Signal): 400 kHz square with random signals such as runts, glitches, staircases, and other signals. Errata: The auxiliary signals TP2, TP20 and TP21 are actually as follows: TP2 = Eyeclk TP21 = Eye Data TP20 = Cheat	Frequency: 400 kHz Amplitude: 4.0 Vpp Anomaly repetition: approx 1 per 750 ms
TP20	Mixed signal “Cheat”	TTL pulse indicating the presence of an anomaly
TP3	AMI 2 Mb/s An alternate mark inversion signal	Frequency: 2.0 Mb/s Amplitude: 4.0 V pk-pk T1.102 DS1A Mask Telecom Trigger: Isolated +1 Isolated -1 Eye Diagram
J2	Time Stamp Out	A varying exponential signal to display a unique waveform for each frame in a FastFrame sequence
TP93	AMI “cheat” signal	TTL pulse indicating the presence of an anomaly
J3 and J9	Logic Analyzer connectors for a LASIV probe	125 MHz, 12 bit parallel signal with ECL (500 ps) edges
J19 and J22	Logic Analyzer Test Point	A specially conditioned signal derived from J3 and J9
J12	USB 2.0 signals The connector is terminated with 100 ohms at the header (use a Hi-Z probe)	480 Mbits/s Vhigh = +400 mV Vlow = 0.00 V Vdifferential - ±400 mV (800 mV pp)
J41	USB Output Clock	3.3 V TTL, 24 MHz
J16	Low Jitter 125 MHz Clock Signal	Frequency: 125 MHz Amplitude: LVPECL Rise/Fall Time: 900 ps Jitter < 6 ps rms
J15	Low Jitter 132 MHz Clock Signal	Frequency: 132 MHz Amplitude: LVPECL Rise/Fall Time: 900 ps Jiter < 6 ps rms
J17	Recovered Clock for the 1.25 Gb/s or 0.625 Gb/s signal	1/10 the serial data frequency of J7. Either 125 MHz or 62.5 MHz depending on the setting of J8.

Table 1: Signal Specifications (Cont.)

Signal		Specification
J10	Recovered Clock for the 2.5 Gb/s Fast Rise Signal	1/20 the serial data rate or 125 MHz
J2880	Voltage on the current loop circuit board run	

Probe Connections

Special connections are included to connect the following probes: P6330, P6248, P7330, P6245, P6249, P7260, and LASI–V

Applying Power to the Training Board 2

Training Board 2 requires a 12 V, 1 A power supply. The power input jack, see Figure 3 on page 3, requires the equivalent of a Switchcraft S760 2.0 mm plug with the center conductor positive.

Compatible power supplies are: the Tektronix part number 119-4812-01, Ault PW118KA1202F02 and the Astrodyne SPU15A-3.

Detailed Signal Description

Fast Edge, J11 and J14

A 2.5 Gb/s 8b/10b encoded serial data stream with sub 100 ps edges.

Description

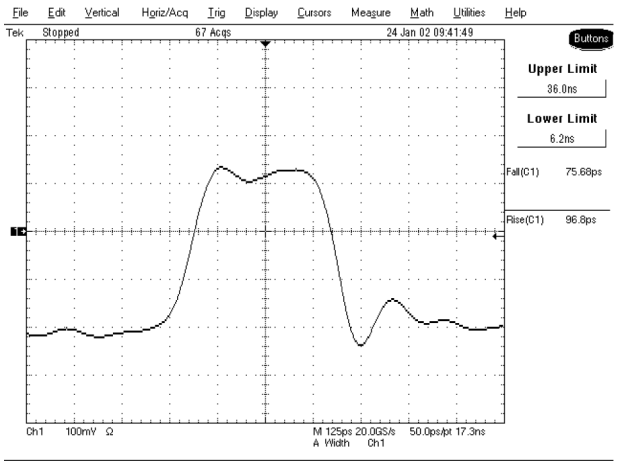
This signal is a differential data stream at the 2.5 Gb/s data rate. The signal level is from an RSECL logic device. This is currently the fastest logic family that is commercially available. The data is generated from a 7-bit pseudorandom sequence generator. A 125 MHz recovered clock is available on J10. The output level of the signal is one schottky diode drop below the RSECL logic levels and was not AC coupled because of the signal degradation that would have occurred from board mounted coupling capacitors. External coaxial AC coupling capacitors such as the Tektronix part number 015-1013-00 SMA DC Block, or the 015-0221-00 BNC DC Block can be used if desired to remove this offset.

Intended Demonstrations

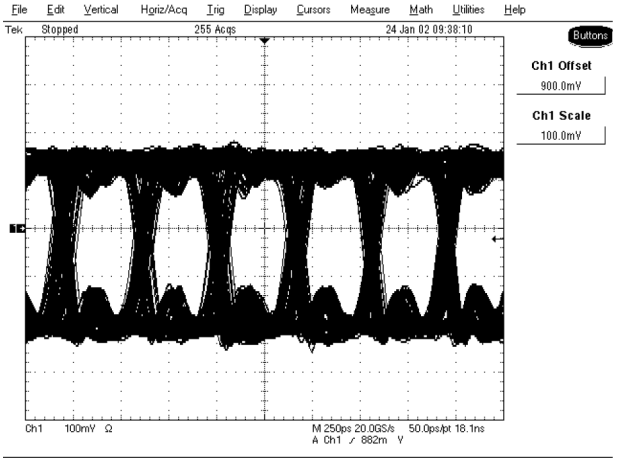
High Speed. This signal was designed to demonstrate the need for fast oscilloscope risetimes. This signal is produced with "off the shelf" logic that is now being produced with extremely fast edges. Signal integrity issues such as overshoot and ringing are also increasingly important to measure since signal defects are very easy to generate with signals that have fast edges such as these. Use Advanced – Width triggers to stabilize the display on the 7-bit pseudorandom sequence.

Communication Signals. This signal is also modulated as a 2.5 Gb/s communication signal. This is the type of signal that would be seen in one of the new serial bus standards such as Infiniband or 3GIO. This signal could be used to demonstrate clock recovery, mask testing, etc.

Probe Connections. Special circuit board run shapes have been included to connect the latest probes to these circuits. The rectangle shaped pads are ground points to minimize loop area of the probe's ground connection.



Fast Edge Tr, Tf Measured with a TDS6604



2.5Gb/s Eye

Figure 4: Fast edge and eye diagram

1.25 Gb/s or 625 Mb/s Signals, J7 Electrical and J23 Optical

Description

This signal is generated from a 7 bit pseudorandom sequence generator at either the 1.25 Gb/s or 625 Mb/s data rate. The rate is selectable by a jumper installed on J8.

Intended Demonstrations

This signal is a general-purpose communication signal that can be used to demonstrate clock recovery, mask testing and serial triggering.

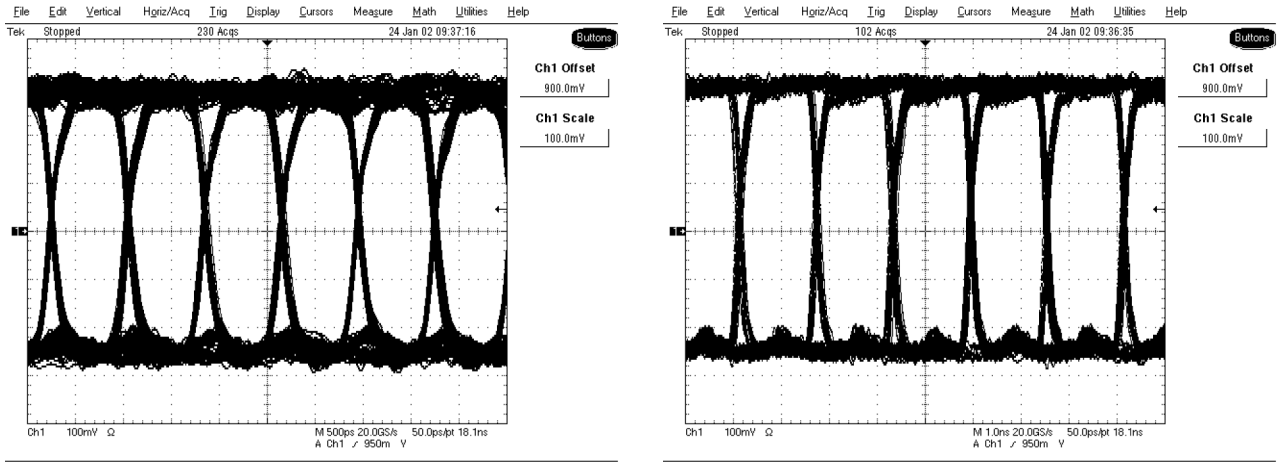


Figure 5: Eye diagrams

Optical Small Form Factor Transceiver Module Connectors, J23 and J28

Two small form factor (SFF) connectors are available. One is connected to the 2.5 Gb/s data rate and the other is connected to the 1.25/0.625 Gb/s data rate. Any transceiver that uses 3.3 V and can accept the indicated data rates can be used in the module socket.

Low Jitter SAW oscillators

Two available oscillator jitter measurements, 125 MHz and 132 MHz. These oscillators have less than 6 ps rms jitter.

Use these signals for Jitter Analysis demonstrations.

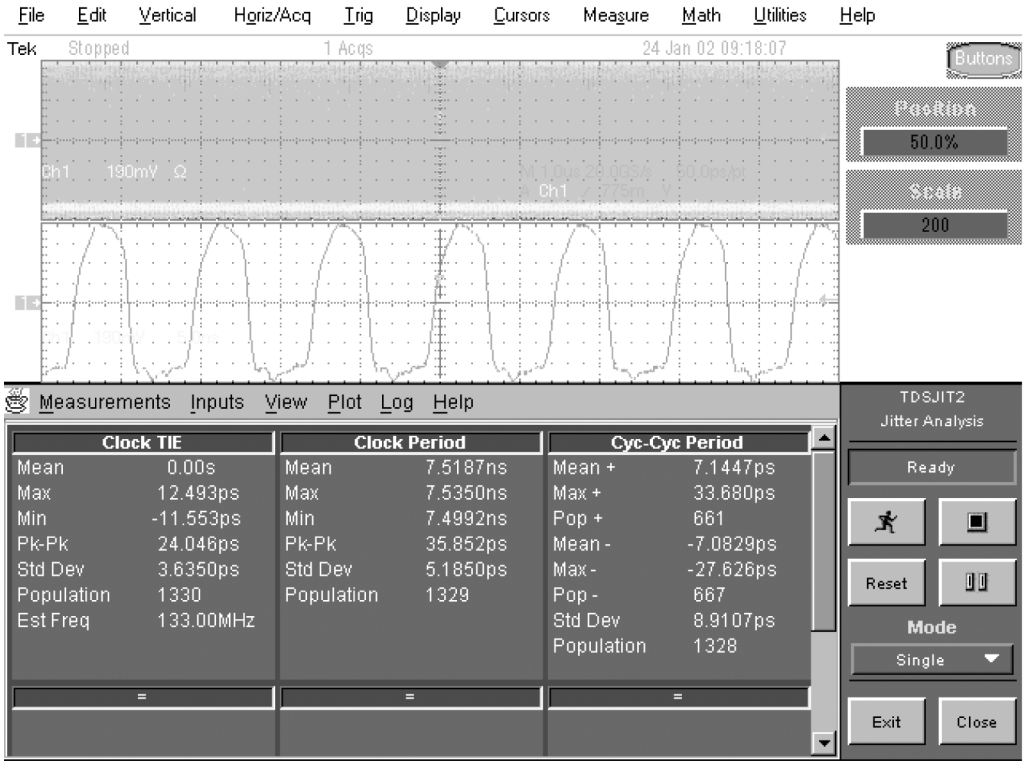


Figure 6: Jitter analysis demonstrations

Clean Edge Signal

This signal steps from –0.25 V to 0.0 0V at a rise time of about 270 ps. There is very little overshoot or ringing on the waveform.

This signal is intended to be used to demonstrate signal fidelity. This signal must be terminated into 50 ohms, even when a probe is used on the “probe point” circuit board pads.

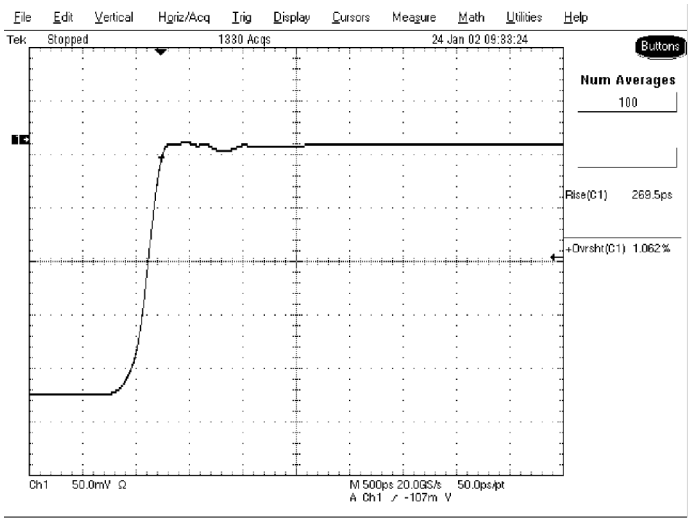
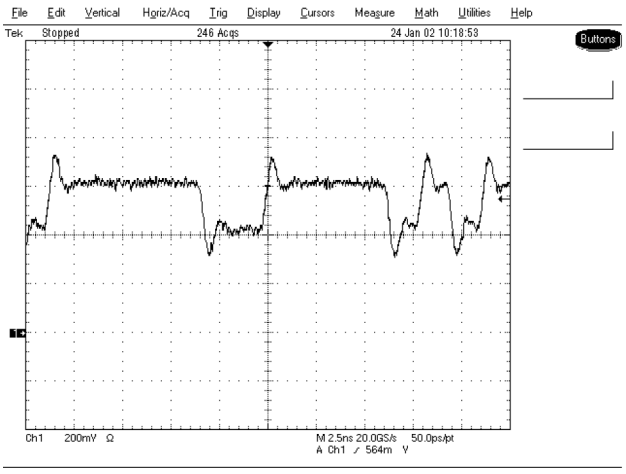


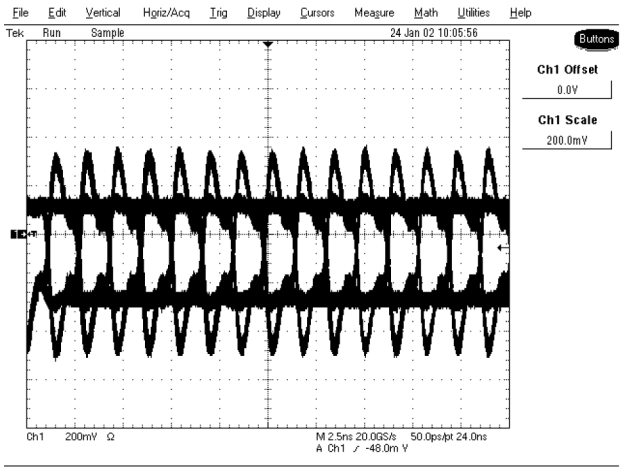
Figure 7: Signal fidelity

LVDS Signal

LVDS level signals are available on J18. These signals follow the signaling rate (1.25 Gb/s or 625 Gb/s) that is selected on J8. Overshoot can be removed by inserting an optical module into the 1.25/0.622 Gb/s receptacle J23.



LVDS Single Sample

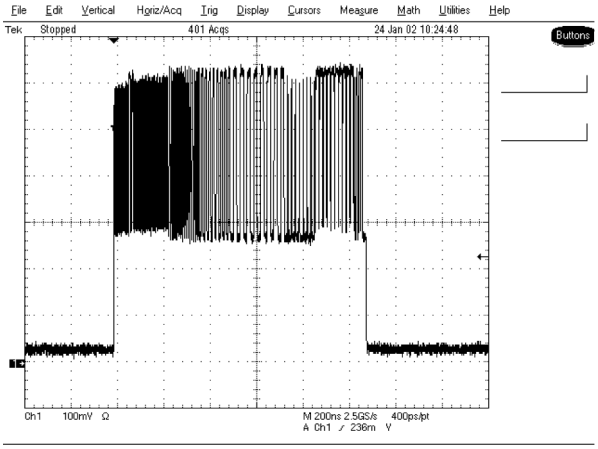


LVDS “Eye”

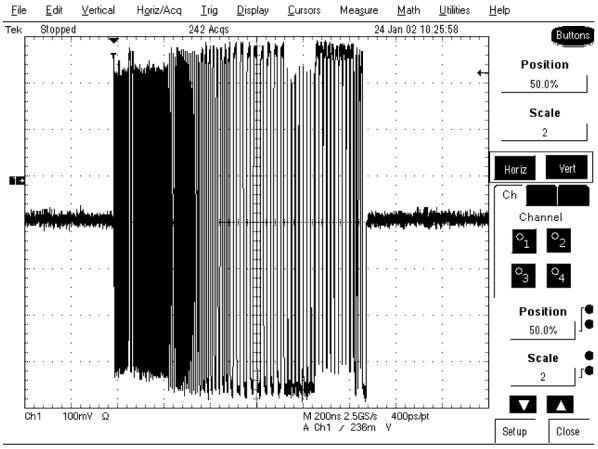
Figure 8: LVDS signal

USB 2.0 Test Packet

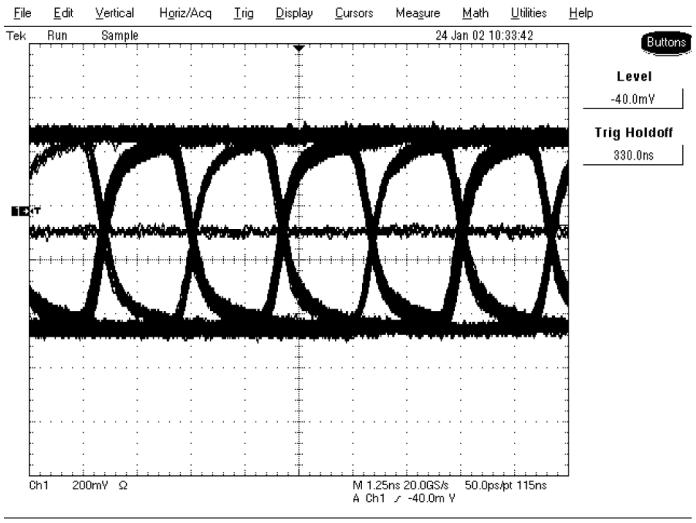
This signal is a differential USB 2.0 signal transmitting the test mode “Test_Packet” signal defined in section 7.1.20 of the Universal Serial Bus Specification Revision 2.0.



USB 2.0 TBST Packet
“Single Ended”



”Differential”



“Eye”

Figure 9: USB 2.0 test packet

Logic Analysis Probe Signals

Description

The 2.5 Gb/s signal, see Figure 9, on page 12, is recovered and de-serialized to form a 16 bit parallel output. This output is routed about 3 inches across the board. A TLA style connector, the “LASI-V” is present at the beginning and at the end of the 3 inch signal route. Some of the signals have intentional shorted stubs added to emulate circuit routing problems. Other signals have up to 9 inches of additional routing length added to mismatch delays. The edge speed of the output is about 500 ps.

Intended Demonstration

This signal was designed to show the ability of our latest logic analyzers to easily display an analog waveform from any of the displayed logic signals. Defects on the signal will be easily seen on the analog waveform and can point to why an incorrect logic signal occurred.

J24 and J25 Arbitrary Waveform Generator Input

These inputs drive specially shaped circuit board runs that out latest probes can connect to. J26 can be used to connect the CT6 current probe to these signals. An arbitrary waveform generator, or any generator including the other Training Board 2 signals, can be cabled to these inputs. There are no active components on these traces. J24 and J25 connect to 50-ohm transmission lines and terminate in 50-ohm resistors.

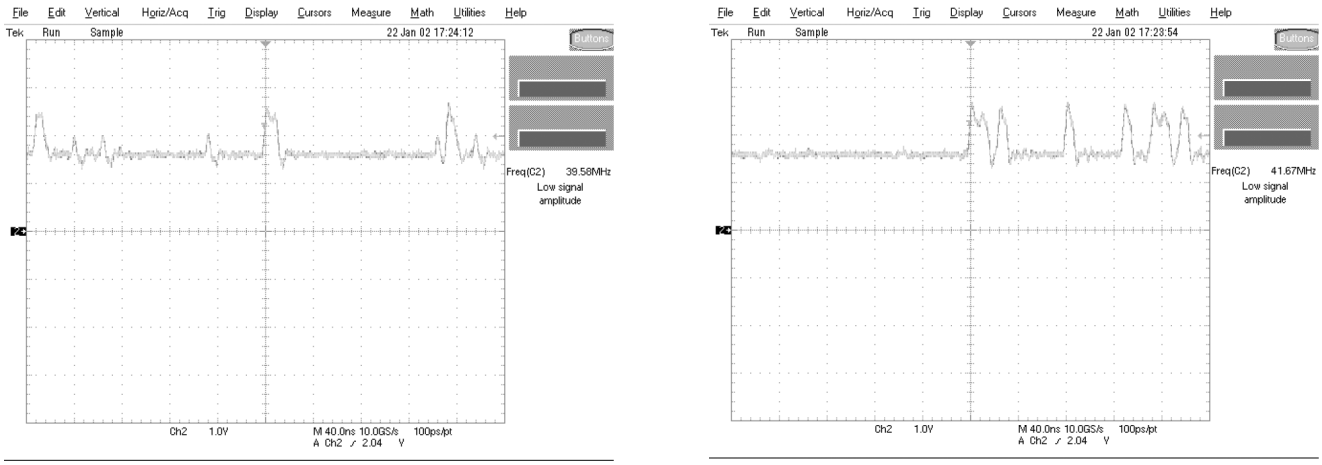


Figure 10: 24 and J25 arbitrary waveform input

Switching Power Supply Signals: V SWITCH, I SWITCH

The V SWITCH and I SWITCH signals are derived from the board's switching power supply. This power supply switches at about 260 kHz. These signals were included to demonstrate the oscilloscope's current, voltage and power measurement capabilities.

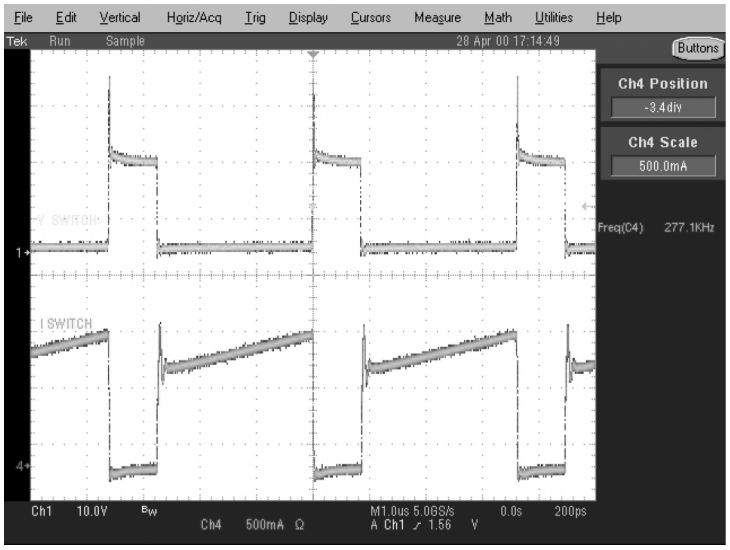


Figure 11: Power supply signals

AMI Signal, Test Point TP3

AMI simulates an "alternate mark inversion" signal at the DS1A data rate (2.048 Mb/s). This signal will look like the following Figure.

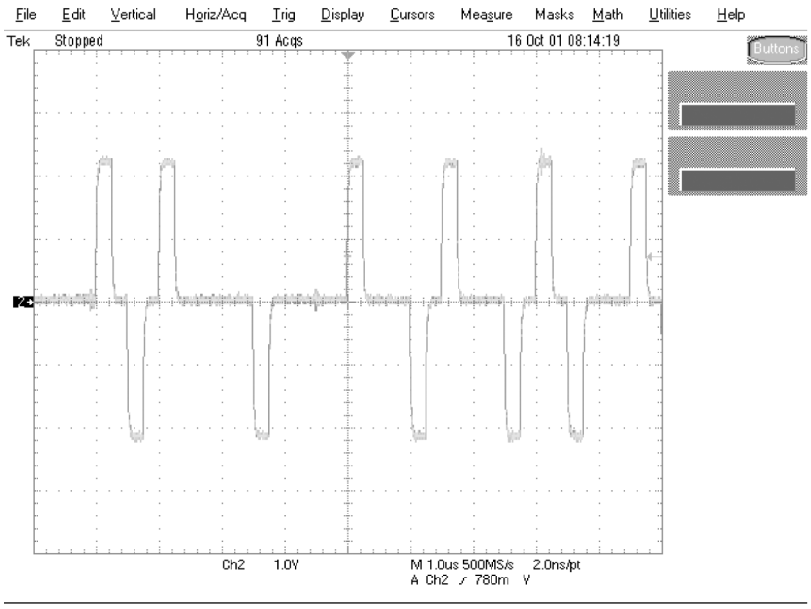


Figure 12: AMI signal at TP3

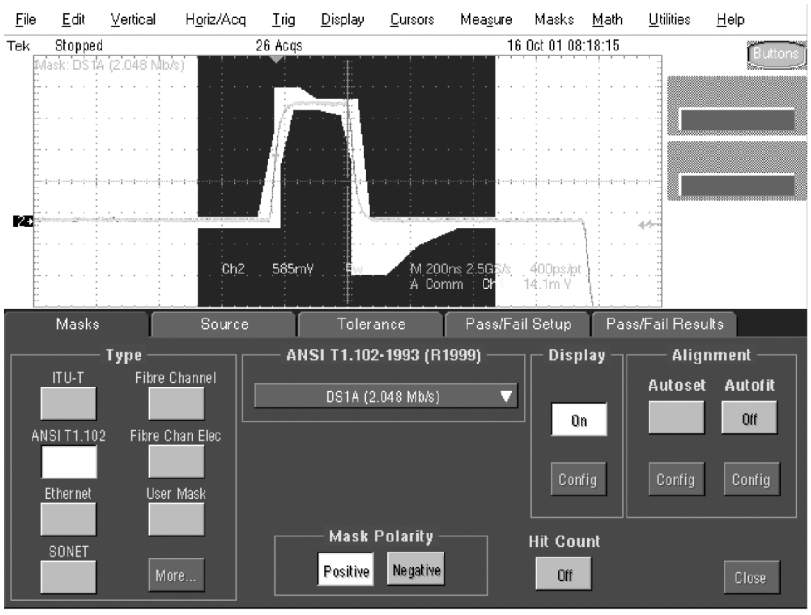


Figure 13: AMI signal in the ANSI T1.102 Mask

This signal also has built in anomalies that are useful for demonstrating Instavu.

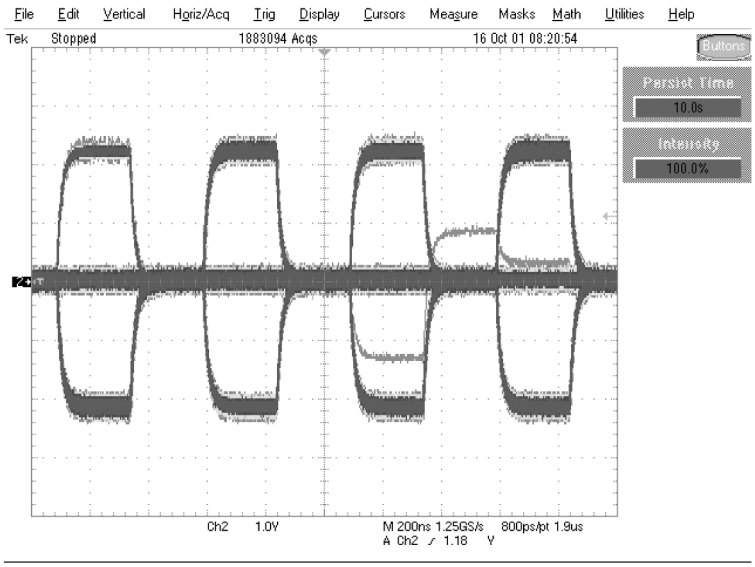


Figure 14: AMI signal and Instavu

Mixed Signal Waveform

Mixed signal is a 400 kHz waveform with a number of intermittent anomalies as shown in Figure 15, on page 17.

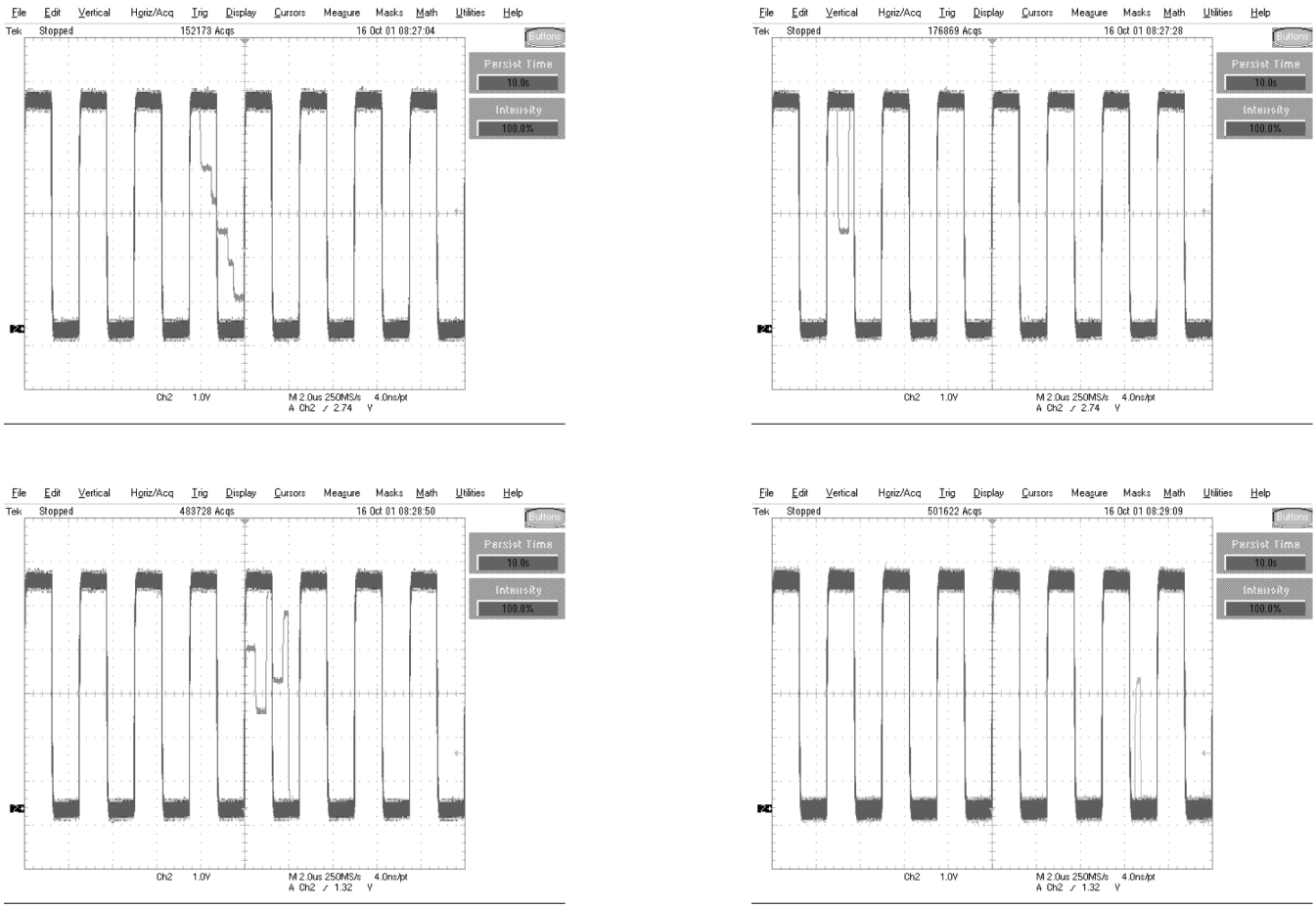


Figure 15: Mixed signal waveform

Staircase

The staircase waveform is a 687 Hz waveform that steps every 164 μs (6.1 kHz). Noise is added to the waveform to demonstrate HiRes. A fast negative going glitch exists at the end of the third step to demonstrate advanced triggering. This is difficult to trigger on because of the presence of noise. Normal glitch triggering will not work very well. One way to trigger on this pulse is shown in Figure 16, on page 18. Finally, intermittent glitches and double steps exist in the waveform to demonstrate FastAcq.

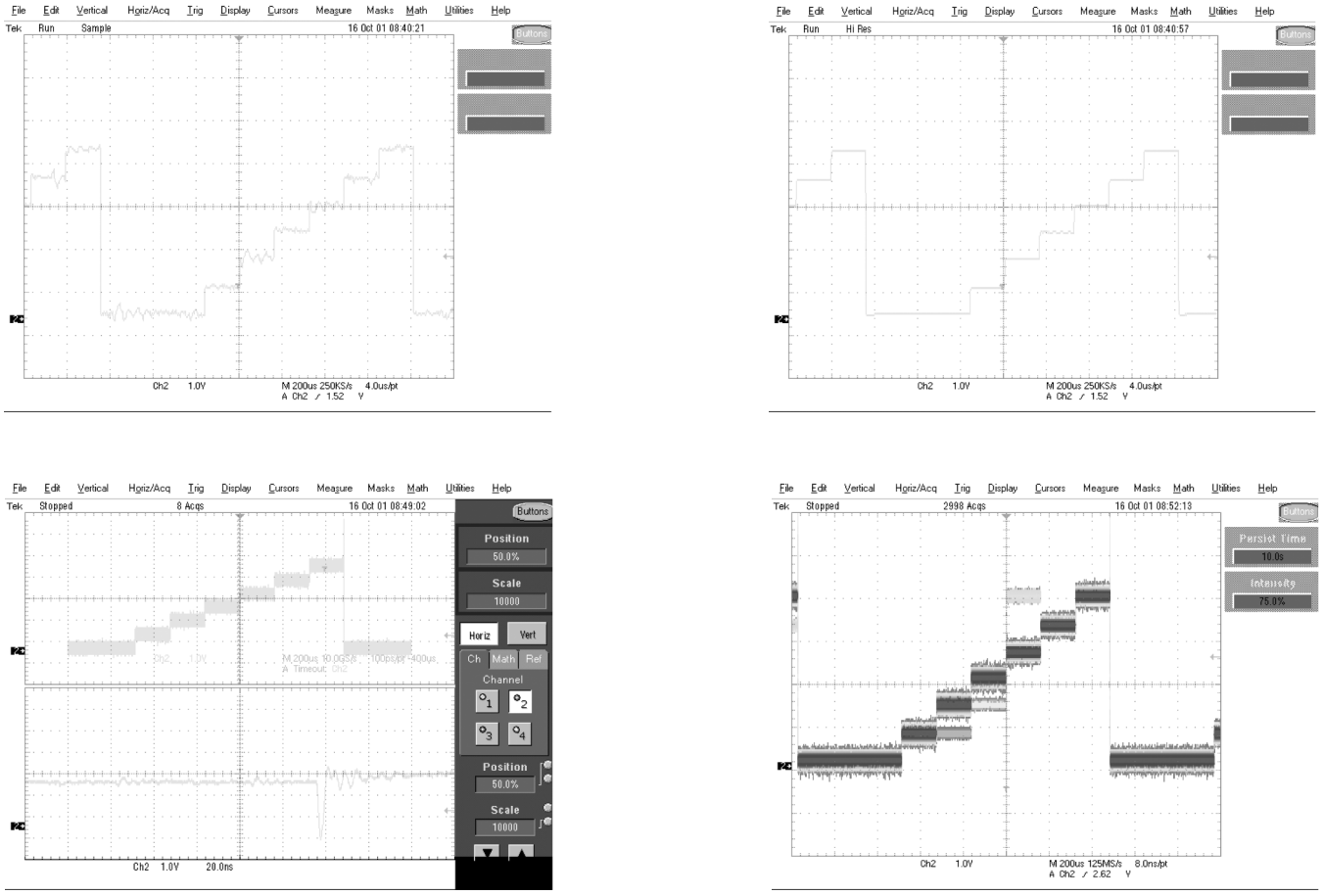


Figure 16: Staircase